Computational Sensors

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Abstract

This report is a result of a workshop on Computational Sensors that was organized and held at The University of Pennsylvania on May **11-12, 1992.** It presents a summary of the state of the **art** in computational sensors and recommendations for future research programs. Approximately **40** people were invited from academia, government, and industry. The workshop hosted several key presentations and followed them with group discussion and summary sessions.

Traditionally, sensory information processing proceeds in three steps: transducing (detection), read-out (and digitization), and processing (interpretation). Micro-electronics technologies have begun to spawn a new generation of sensors which combine transducing and processing on a single chip - a computational sensor.

A computational sensor may attach analog or digital **VLSI** processing circuits to each sensing element, exploit unique optical design or geometrical arrangement of elements, or use the physics of the underlying material for computation. Typically, a computational sensor implements a distributed computing model of the sensory data, including the case where the data are sensed or preprocessed elsewhere. Combining computation and signal acquisition into a single chip results often in not only performance improvement but also totally new capabilities that were not previously possible. Finally, the workshop made several important recommendations.

1. Create a research and development program in computational sensors. The program must have the following characteristics:

   - Interdisciplinary - the program must include sensing, algorithms, **VLSI,** material, and applications;
   - Multi-modal - the program must deal with not only the image or visual modality, but also with other sensing modalities including tactile, acoustic, pressure, acceleration, chemical, and so on;
   - Prototyping-oriented - individual projects under this program must be oriented toward producing working prototype devices or systems;
   - Applications - individual projects must identify potential applications and possible avenues of technology transfer to real world applications.

2. Improve the infrastructure for research and development of computational sensors:

- Fabrication facilities - MOSIS (or similar facilities) must be expanded to include technologies for optical and mechanical sensor development;
- Tools - Tools for designing and testing computational sensors can be far more complicated than they are for standard VLSI design. Standardization, and library and tool development are essential;
- Education - Hands-on experience must be provided to graduate students;
- Networking and workshops - Researchers in computational sensors, by its nature, are scattered in multiple fields, and mechanisms; workshops and consortiums must be developed to bring them together.

1 Introduction

Traditionally, sensory information processing proceeds in three steps: transducing (detection), read-out (and digitization), and processing (interpretation). Micro-electronics technologies has begun to spawn a new generation of sensors which combine transducing and processing on a single chip - a computational sensor.

A computational sensor may attach analog or digital VLSI processing circuits to each sensing element, exploit unique optical design or geometrical arrangement of elements, or use the physics of the underlying material for computation. Typically, a computational sensor implements a distributed computing model of the sensory data, including the case where the data are sensed or preprocessed elsewhere. Combining computation and signal acquisition into a single chip results in often not only performance improvement but also totally new capabilities that were not previously possible.

Recognizing the importance and potential of computational sensors, Oscar Firschein, DARPA SISTO, requested us to organize a workshop to bring together developers and users of computational sensors. The workshop was to define the state of the art, discuss the issues, and identify promising approaches and applications for this new technology. The workshop was held at The University of Pennsylvania on May 11-12, 1992. Approximately 40 people were invited from academia, government, and industry. The workshop hosted several key presentations and followed them with group discussion and summary sessions. This workshop report presents a summary of the state of the *art* in computational sensors and recommendations for future research programs.

In Section 2 we discuss opportunities for computational sensors. Some computational sensor examples *are* reviewed in Section 3. Technologies, issues, and limitations are considered in Section 4. Section 5 discusses algorithms for computational sensors. Recommendations for future programs are given in the concluding section. The appendix includes a bibliography of computational sensing created with input from the workshop participants.

2 Opportunities

In machine vision, the basic approach has been to use a TV camera for sensing, to digitize the image data into a frame buffer and then to process the data with a digital computer. Apart from being expensive, large, heavy, and power-hungry, this sense-digitize-and-then-process paradigm has fundamental performance disadvantages. A high bandwidth is required to transfer data from the sensor to the processor. The parallel nature of operands captured in a 2D image plane is not exploited. Also, high latencies due to image transfer and store limit the

usefulness of this paradigm for high-speed, real-time applications. Combining processing on silicon wafers together with detectors will eliminate these limitations, and have the potential to produce a visual sensor of low-cost, and low-power with high-throughput and low latency.

The potential for integrating the transducing and processing of signals has been recognized for some time, but in the past, research and development in this area was driven mostly by curiosity or special use. Today, however, the advancement of VLSI and related technologies provides opportunities for us to harness this potential in new, broad, practical applications in image understanding, robotics, and human-computer interfaces. Most importantly, VLSI technologies have become available and accessible to the sensor application community where we have recently observed a growing body of research in computational sensors.

Several computational sensors have been fabricated and demonstrated to perform effectively. Analog vision chips have been demonstrated which can compute an image motion vector, or continuously compute the size and orientation of an object. Three dimensional range sensing has been performed at a rate of 1000 frames per second using a chip containing an array of cells each capable of detecting and calculating the timing of an intensity profile. Sensor chips that mimic the human's fovea and peripheral vision have been fabricated and used for pattern recognition. Tiny lenses can be etched on silicon to focus light efficiently on a photosensitive area, or even to perform a geometrical transformation of images. Resistive networks and associated circuits on a chip can solve optimization problems for shape interpolation.

Computational sensors are not limited to vision use, but have applications in mechanical, chemical, medical and other sensors. Development of micromechanical pressure sensors and accelerometers has been underway for some time. An air-bag sensor for automobiles could become one of the first successful, mass-produced, low-cost computational sensors. It contains a miniature accelerometer and processing circuits in a chip. Processing could also be combined with micro-chemical sensors to detect water contamination, air pollution, and smells, while micro-medical sensors could measure blood chemistry, flow, and pressure.

Potential applications/markets of computational sensors are abundant:

- robot perception
- industrial inspection
- navigation and automobile
- space

- sensor based appliances
- medicine (e.g. patient monitoring)
- security and surveillance
- entertainment and media
- toy

Development of a computational sensor does not simply mean combining known sensing capability with known processing algorithms. It requires new thinking. Most of the current vision algorithms, for example, are strongly influenced by the fact that image data is provided in a stream and processed by instructions. Also, certain concepts, such as frame rate (ie., considering a certain number of discrete frames per second), are themself artifacts of the sense-digitize-and-then-process paradigm. Instead, a computational sensor *can* and should take advantage of the inherent, two-dimensional nature of the sensory data arrangement, the continuous time-domain signal, and the physics of the media (eg. silicon) itself for processing. This type of new thinking often results in a completely different, more efficient, orders-of-magnitude faster "algorithm". Many of the successful examples mentioned above and in section 3 are the results of such new thinking.

Finally, computational sensors *can* create a fundamental change in the approach to the sensor system as a whole. When a sensor is bulky, expensive and slow, it is not affordable, both economically and technically, to place many of them within a system. The sensor system is forced to be centralized. If computational sensors *can* provide cheaper, smaller, and faster sensing units, we *can* place a large number of sensors throughout a system, such as covering the whole surface of a submersible vehicle. A new opportunity exists to make sensor systems more distributed, reliable, and responsive.

3 Computational Sensors: Some Examples

This section reviews computational sensor architectures that have emerged in recent years:

1. The focal plane computational sensor: Processing is done on a focal plane, i.e. the sensing and processing element are tightly coupled;
2. The spatio-geometrical computational sensor: Computation takes place via the inherent geometrical structure and/or optical properties of the sensor;

3. The **VLSI** computational module: Sensor and processing element are not tightly coupled, but processing is done on a tightly coupled module.

Many existing systems would fall into several of the above categories. Representative examples of each category are presented here.

Although most examples we give are of visual information processing, these considerations and techniques extend directly to measurement over the whole spectrum of electromagnetic radiation. In general, any other "imaging sensors" such as mechanical (e.g. tactile) or magnetic sensors, could also benefit from lessons learned when considering and designing computational sensors for vision applications.

3.1 The focal plane architecture

The focal plane architecture tightly couples processing and sensing hardware—each sensing site has a dedicated processing element. The sensor and the processing element (PE) are located in close physical proximity, thus reducing data transfer time to PE's. Each PE operates on the signal of its sensor. However, depending on the algorithm, each PE may need the signals of neighboring sensors or **PE's.** This concept corresponds to the SIMD paradigm of parallel computer architectures. In computational sensors, the operands are readily distributed over an array of **PE's as** they are being sensed.

Cell Parallelism

Gruss, Carley and Kanade [24] [25] [38] at Carnegie Mellon have developed a computational sensor for range detection based on light-stripe triangulation. The sensor consists of an array of cells, each cell having both a light detector and a dedicated analog-circuit PE. The light stripe is swept continuously across the scene to be measured. The PE in each cell monitors the output of its associated photoreceptor, recording a time-stamp when the incident intensity peaks. The processing circuitry uses peak detection to identify the stripe and an analog sample-and-hold to record time-stamp data. Each time-stamp fixes the position of the stripe plane as it illuminates the line-of-sight of that cell. The geometry of the projected light stripe is known as a function of time, as is the line-of-sight geometry of all cells. Thus, the 3-D location of the imaged object points ("range pixels") can be determined through triangulation. The cells operate in a completely parallel manner to acquire a frame of 3-D range data, so the spatial resolution of the range image is determined solely by the size of the array. In the current CMOS implementation, an array of 28 x 32 cells has been fabricated on a 7.9mm x 9.2mm die.

Keast and Sodini [39] at MIT have designed and fabricated a focal plane processor for image acquisition, smoothing, and segmentation. The processor is based on clocked analog CCD/CMOS technology. The light signal is acquired as an accumulated charge. The neighboring PE's share their operands in order to smooth data. In one iteration, each PE sends one quarter of its charge to each of its four neighbors. The charge meets halfway between the pixels and *mixes* in a single potential well. After mixing, the charge is split in half and returned to the original PE, approximating Gaussian smoothing. However, the segmenting circuit will prevent this mixing if the absolute difference between the neighboring pixels is greater than a given threshold. A 40 x 40 array with a cell size of about 150 x 150 microns is currently being fabricated.

Use of Media Physics (Resistive Grid)

Some algorithms *can* exploit the physics of the VLSI layers to achieve "processing" in a computational sensor. Carver Mead at Caltech has developed a set of subthreshold CMOS circuits for implementing a variety of vision circuits. The best known design is the "Silicon" retina, a device which computes the spatial and temporal derivative of an image projected onto its phototransistor array. The photoreceptor consists of a phototransistor feeding current into a node of a 48 by 48 element hexagonal resistive grid with uniform resistance values R. The photoreceptor is linked to the grid by a conductance of value G. An amplifier senses the voltage between the receptor output and the network potential. The circuit computes the Laplacian of an image, while temporal derivatives are obtained by adding a capacitor to each node.

Another example which exploits resistive grids to achieve signal processing is the blob position and orientation circuit developed by Standley, Horn, and Wyatt at MIT [81] [82]. Light detectors are placed at the nodes of a rectangular grid made of polysilicon resistors. The photo-current is injected into these nodes and the current flowing out of the perimeter of the grid is monitored. The injected photocurrent and the grid perimeter current are related through Green's theorem; based on sensed perimeter current, information to compute the first and second moments of the blob is extracted at 5000 frames/sec. An array of 29 x 29 cells has been fabricated on a 9.2mm x 7.9mm die.

3.2 Spatio-Geometric and Optical Computational Sensors

Some computational sensors are based on the "computation" performed by virtue of the special geometry or optical material of the sensor array.

Log-Polar Sensor

The University of Pennsylvania's log-polar sensor developed by Kreider and Van der Spiegel [45] [46] [71] [75] in collaboration with Sandhi of University of Genova and researchers at IMEC in Belgium has a radially-varying spatial resolution. A high resolution center is surrounded with a lower resolution periphery in a design resembling a human retina. A sensor that has a high spatial resolution area, like a fovea in a human retina, is often termed a foveating sensor. The image is first mapped from log-polar to the Cartesian plane. There is evidence that in biological systems this type of mapping takes place from eye to brain. The authors have shown that transformations involving perspective, such as optical flow and rotation, are simplified with such a mapping. This sensor must be mechanically foveated for a specific region of interest, and current research concentrates on applying this chip to robotics.

Bederson, Wallace, and Schwartz [7] at New York University and Vision Application, Inc. designed a log-polar sensor as well. The VLSI sensor itself is in the process of being fabricated. An additional interesting part of their system is a miniature pan-tilt actuator called Spherical Pointing Motor (SPM) shown. The SPM is capable of carrying and orienting the sensor. It is an accurate, fast, small, and inexpensive device with low power requirements and is suitable for active vision applications.

Another foveating sensor has been designed by Kosonocky, Wilder and Misra at Rutgers University. The objective was to design a sensor whose foveal region(s) will be able to expand, contract and roam in the field-of-view. The chip is, in essence, a 512x512 square array with the ability to "merge" its pixels into regions, and output only one value for each such rectangular "super pixel". The largest super pixel is an 8x8 region. There are three modes of operation. In Variable Resolution Mode, the resolution of the entire chip can be selected from highest to lowest, or anywhere inbetween. The Multiple Region of Interest mode provides multiple active windows, possibly with different resolutions, while reading data out from the rest of the array is inhibited. The third mode is a combination of the first two modes. This third mode would resemble the sampling of a human retina if so programmed. The design permits multiple foveae within the retina. The authors demonstrated significant speed-up in data acquisition for a variety of tasks from industrial inspection to target tracking.

Hexagonal Tessellation

Hexagonal sampling tessellates the frequency plane more efficiently than rectangular sampling.[1] Poussart and Trembley [89] at Laval designed a 200 x 200 array with a hexagonal grid. This chip facilitates parallel access to the data in a particular local neighborhood. For rapid convolution, this local neighborhood is subsampled along three principal axes of the grid, thus reducing the data needed for convolution in the local neighborhood of each pixel. Their MAR (Multi-port Array Photo-Receptor system) performs zero-crossing detection at seven spatial frequencies in 16 milliseconds. Edge detection is computed in real time.

Binary Optics

By etching desired geometrical shapes directly into the surface of an optical material, a designer can produce optical elements with properties that were previously impossible to achieve. This method, called binary optics, can perform simple optical processing before the light is detected.

As VLSI microlithographic techniques have advanced, inexpensive fabrication of binary optical devices has become possible [91]. Veldkemp of Lincoln Lab at MIT has developed a micro lens array in which each lens is only 200 microns in diameter. One application of such an array would be to focus light onto tiny photodetectors thus saving silicon area for processing hardware. Some of the first applications of the idea are already on the market: Hitachi FP-C10 HI-8 video coders use a micro-lens array CCD, and the Sony XC-75 video camera doubles the sensitivity to f8 @ 2000Lux using their HyperHAD CCD structure which uses micro lenses. In addition, binary optics devices have been applied to automatic target recognition and space applications.

McHugh of Hughes Danbury Optical Systems experimented with binary optical techniques and found that they can generate virtually any transformation of an optical wave front. The first application that used this new capability was a binary optical component that optically mapped the log-polar plane to the Cartesian plane. This device, in effect, samples images at log-polar resolution and optically transforms them for sensing on a Cartesian grid. This way an optical log-polar foveating sensor is produced, while the mapping to the Cartesian plane has become "free of charge".

[1] Nature prefers hexagonal sampling, which is actually found in the mammalian retina.

Color and Polarization

Wolff at Johns Hopkins University uses liquid crystal polarizers whose polarization angles are electronically controlled [98]. It has been reported that by eliminating mechanical rotation of filters, switching time between different polarization angles is reduced, and accuracy of results is improved. Wolff hopes to build polarization cameras with polarizers in each element of the CCD array for acquisition of polarized images in real-time. For specularity detection, material classification and object recognition, color and polarization carry independent and complementary information: polarization for specularity, and color for diffuse surfaces and light sources. Sensors for real-time combination of both color and polarization images will add rich information to vision systems.

3.3 Computational Modules for Sensory Information Processing

While not strictly a computational "sensor", there is a class of computational modules for sensory information processing which exploit VLSI technologies in a similar manner as computational sensors.

These computational modules are useful when there is not enough space on a single chip to accommodate complex PE's, or the data to be processed comes from other modules.

Smoothing and Optimization by Resistive Networks

At Caltech, several regularization techniques have been implemented on-chip. For example, consider the problem of fitting a 2D surface to a set of sparse, noisy depth measurements by imposing a "smoothness" constraint. This method produces quadraticly varying functions. This can be solved using simple linear resistive networks by virtue of the fact that the electrical power dissipated in linear networks is quadratic in the current or voltage [69].

Mapping 2D motion algorithms onto analog chips has turned out to be surprisingly difficult. A robust motion detection circuit implemented in analog VLSI has yet to be demonstrated, but early effort has been made by Tanner at Caltech [86] [87]. He successfully built and tested an 8x8 pixel chip that outputs a single uniform velocity averaged over the entire image. His chip reports values of x and y velocity which minimize the least square error in the image brightness constraint equation.

Bair and Koch have successfully built an analog VLSI chip that computes zero crossings of the difference of Gaussians. It takes the difference between two copies of an image. supplied by a 1-D array of 64 photoreceptors, each smoothed by a separate linear first-order resistive network, and reports the zero-crossings in this difference [6]. This implementation

has the particular advantage of exploiting the smoothing operation naturally performed by resistive networks, and therefore avoids the burden of additional circuitry. The network resistance and the confidence of the photoreceptor input are independently adjustable for each network. Also, an adjustable threshold on the slope of zero-crossings can be set to cause the chip to ignore weak edges due to noise.

Binary line processes which model discontinuities in intensity within the stochastic framework of Markov Random Fields provide a method to detect discontinuities in motion, intensity, and depth. This is achieved by selectively imposing the smoothness assumption. Harris and Koch have invented the "resistive fuse", which is the first hardware circuit that explicitly implements line processes in a controlled fashion [29]. Like a normal house fuse, a resistive fuse operates as a linear resistor for small voltage drop and as an open-circuit for large voltage drops. A 20x20 rectangular grid network of fuses has been demonstrated for smoothing and segmenting test images which are scanned onto the chip.

Pyramid

Van der Wal and Burt at David Sarnoff Research Center developed a VLSI pyramid chip PYR [92]. Combined with external framestore, the PYR chip is capable of computing Gaussian and Laplacian pyramid transforms simultaneously. These transforms consist of Gaussian filtering and consecutive subsampling, and, for Laplacian, image subtraction. The Chip has a separable 5 by 5 filter and four 1024-sample-long delay lines. Each filter tap has a preassigned set of possible values. Coefficient values from this set can be changed under software control. PYR has special features such as double precision, double sample density, image border extension and automatic timing control. At 15MHz a single chip can compute Gaussian and Laplacian pyramids at 44 frames/second for 512 by 480 images. PYR is implemented in digital VLSI using the CMOS standard cell library from VLSI Technology, Inc. Digitized image samples pass through the chip sequentially, in raster scan order.

4 Issues

Successful development of a computation sensor relies on careful consideration of several issues including:

- choice of the circuitry: digital vs. analog electronics, choice of sensors with respect to spectral bandwidth (color) and polarizers,

- choice of an algorithm,
- state-of-the-art VLSI,
- prototyping infrastructure: design tools and fabrication facilities,
- applications,
- education, workshops/networking, literature.

All of these issues are discussed in the following sections.

4.1 Analog vs. Digital

Both digital and analog circuits *can* be implemented using **VLSI** technology. The analog approach can be conceptually divided into continuous-time (unclocked) and discrete-time (clocked) processing. The choice of technology depends on the particular application, but several general remarks are in order. Compared to digital, the traditional disadvantage of analog electronics is its susceptibility to noise, yielding low precision. The source of this noise can be on-chip switching electronics which require special considerations for hybrid designs. Also, analog electronics do not provide efficient long-term storage; typical storage times are about one second. On the other hand, digital processing requires A/D and D/A conversion, which usually imposes limitations on total circuit speed. Analog electronics are characterized by:

- high speed,
- low latency,
- low precision (typically 6 to 8 bits),
- short data storage time (typically 1 second),
- sensitivity to on-chip digital switching; and
- a long design and testing process.

In general. analog hardware takes less chip area than digital mechanisms of the same functionality. Most participants at the workshop were experts in analog circuitry which

seems to be preferred; however, many recognized the importance of digital electronics for computational sensing.

Analog VLSI offers two interesting advantages for computational sensor design. First, the physical properties of the solid-state layers and devices can sometimes be exploited to yield elegant, new solutions. One such example is to exploit the physics of a resistive sheet (or dense grid) to compute desired quantities.

The second interesting advantage of analog VLSI is charge-domain processing, best exemplified by CCD technology, which offers an area-efficient mechanism for transferring data. In addition, creative processing schemes can be developed to process the data in charge-domain as it is transferred. CCD technology has already provided several useful examples of integrated sensing and signal processing.

4.2 Algorithms for Computational Sensors

While the VLSI computational sensor offers exciting opportunities, one must be careful in deciding which algorithms or applications will benefit from such an implementation. At the present state of technology, successful design of working VLSI circuits, especially analog ones, is a lengthy process.

Algorithms must be carefully selected or invented to match the architecture to the circuitry for maximum performance - there are definite limitations on circuitry and architectures. Circuitry has limited precision and storage. Until technology allows much denser circuits (or 3D structures) for example, there is not enough room to fabricate a complex PE at each photo site.

Simple cell-parallel algorithms that detect local cues or integrate local information over time or multiple channels (eg. spectrum) at each cell are most ideal.

When a complex PE is required, processing and sensing can take place on separate, but tightly coupled (preferably on-chip) modules. The cost of transferring data must be minimized in order to justify the use of VLSI over conventional computer systems. CCD row-parallel transfer is one way to perform the transfer at a reasonable speed. Also, some algorithms do not directly exhibit parallelism in the focal plane; they often require significant local data storage at each PE. In stereo algorithms, for example, optical signals are to be combined from two different focal planes. In this case, data are read out and processed on a separate computational module.

There are optimizations and other techniques that map naturally to physical processes in silicon; such as relaxation processes implemented on resistive grids. The advantage of these physics-based processors over computer implementation is that they minimize a multi-dimensional energy function by reaching a stable state of a continuous-time sys-

tem, potentially reducing round-off error and numerical instability from which an iterative solution by a digital computer may suffer.

In summary, the following are some general characteristics of algorithms which are good candidates for computational sensors implementation:

- Algorithms that are simple and robust to noise, and are based on sensor or cue integration
- Algorithms that exploit a significant level of parallelism without requiring significant storage capacity, wafer real estate, or inter-processor data transfer.
- Algorithms that map naturally to physical processes encountered in semiconductors,
- Algorithms that could exploit the intercommunication and propagation afforded by charge-transfer, surface acoustic waves, and optical properties.

4.3 VLSI Technology

CMOS, Bipolar, and BiCMOS are the most available VLSI technologies. CMOS is characterized by very dense packaging, low power consumption, and high input impedance. Good switching properties make it well suited for digital, switching, and hybrid circuits. It is widely accessible and relatively inexpensive technology. CCD's are implemented in MOS technology.

Bipolar technology is characterized by low noise and fast circuitry, but consumes more power and takes more substrate real estate. It is not as accessible to the wider research community as it probably should be.

BiCMOS combines the advantages of both CMOS and Bipolar technologies.

Semiconductor material other than silicon is also available. GaAs compounds yield very high speed circuitry and are well suited to electro-optical applications. GaAs technology is less available, however, and is considerably more expensive.

The trend in VLSI is toward smaller device geometries. This produces both smaller and faster digital circuits and hence more functionality per unit area. This scaling, however, is not as beneficial to analog circuitry as to digital. Most active devices are designed at a given size and scaling and would not preserve desired functional features after a scale change. Analog MOS circuits benefit more from improvements in fabrication process quality. Factors such as oxide quality and thickness, or tighter control of threshold voltages would greatly benefit analog circuit performance.

Great interest has been shown in 3D VLSI. One possibility is optical signal communication between stacked chips. This could be accomplished with the availability of silicon-compatible semiconductor emitters and IR detectors [88]. This technique would also require and exploit integrated optics capability such as binary optics. Alternatively. a conducting feedthrough could be developed for making distributed point-to-point electrical connections [68].

Micro fiber-optics could be used to route data in parallel from module to module. The optical approach has the advantage of possible optical processing during the data transmission itself, but has the disadvantage of high power consumption and heat dissipation. This technology has not been developed far enough to become accessible to the wider research community.

4.4 Applications

As VLSI technology advances and becomes accessible to a wider research community, a number of ideas that combine sensing and processing on a chip are emerging. Many attempts, however, are too quick to postulate miraculous chips and systems which have little chance of ever working.

Several successful examples of computational sensors have been driven by applications, and the workshop participants have agreed that this will remain true for most successful developments. A truly successful "marriage" of sensing and computation *can* be done only by careful analysis of application requirements in conjunction with implementation technologies.

While a wide variety of applications are conceivable, the following are potential applications that have been suggested during the workshop:

- A high resolution camera (2000 x 2000 and up).
- Face recognition for credit purchase, security, and human-computer interfaces.
- *An* inexpensive anti-collision stereo sensor for automobiles.
- Motion detection and tracking for automobiles, security, and human-computer interfaces.
- Automatic local brightness adjustment of images.
- Tactile sensors for material handling.

- Insect robots for the toy industry.
- High-speed industrial inspection, chip reticle alignment.
- Document understanding and optical character recognition.
- A light-weight amacronic sensor/display device for virtual reality.
- Image compression for home video appliances.
- Medical sensors/implants.
- Automatic target recognition - signal preprocessing for specialized sensors (gain, bias, filtering) and multi-sensor integration. An example is a computational sensor to perform the functions of detection, inscan calibration, and output multiplexing of FLIR.
- Space robotics for orbital replacement, satellite retrieval, and planetary exploration.
- Remotely and automatically piloted vehicles - sensors to make UGV, AAV, AUV low cost.

4.5 Prototyping Infrastructure

Design tools

An issue which received unanimous agreement among workshop participants is the lack of analog VLSI design tools equivalent to those for digital design. These tools include design aids from layout to testing, including extraction, verification and simulation. Analog circuits are more sensitive to parasitics than digital circuits. Accurate techniques for including these parasitics in the extracted files would reduce the number of design iterations due to unexpected circuit behavior.

Analog modeling and simulation capabilities are still inadequate. Much of the attention in modeling is directed at the effects of extremely short channel lengths on MOS transistor operation. Analog design rarely uses minimum size transistors, but is more critically dependent upon operating under a different bias condition: subthreshold and saturation regions. The proper modeling of bias-dependent capacitances is critical for modeling circuit dynamics and stability. There is little or no support for simulating charge-domain devices like CCD's. Statistical modeling is an important predictive element of analog design, providing assurance that the resulting circuits will meet the prescribed design constraints.

Without it, a circuit may be functional and within specifications for a given process model, but actual process variation may result in an out-of-spec or inoperable circuit.

It has been noted that a data book for standard analog cells would be very useful. While it will be more difficult than the digital domain, it is necessary to develop a library of standard building blocks of compatible electronic and sensor components with which one can design a new computational sensor.

Fabrication Facilities

The MOSIS Service is a prototyping service offering fast-turnaround standard cell and full-custom VLSI circuit development at very low cost. The MOSIS Service, begun in 1980, provides fabrication services to government contractors, agencies, and university classes under the sponsorship of the Defense Advanced Research Projects Agency (DARPA) with assistance from the National Science Foundation (NSF). MOSIS has developed a methodology that allows the merging of many different projects from various organizations onto a single wafer. Instead of paying for the cost of mask-making, fabrication, and packaging for a complete run (currently between $50,000 and $80,000) MOSIS users pay only for the fraction of the silicon that they use, which can cost as little as $400. Initially, the MOSIS user-base was primarily university and government users. MOSIS' success in serving this group of users led, in recent years, to a natural expansion into the industrial sector, with rapidly growing use of MOSIS by commercial companies. MOSIS foundries have also taken advantage of the frequent prototype runs for their own needs as well as those of their clients. MOSIS is located at the Information Sciences Institute of the University of Southern California (USC/ISI) in Marina del Rey, California

The MOSIS program has been a successful mechanism for promoting VLSI applications. MOSIS' ease of access, quick turnaround, and cost-effectiveness have afforded designers opportunities for frequent prototype iterations that otherwise might not even have been considered. With MOSIS' low cost for "tiny-chip" fabrication, silicon can be used as a rapid prototyping vehicle. Small functional building blocks can be easily fabricated and tested before too much time is invested in building and integrating a full system. Furthermore, many ideas and needed intuition can be gained through "playing" with these actual working chips. Successful designers of existing functional computational sensors have reported that silicon prototyping, combined with higher level algorithm simulation, has proven to be a useful system-building approach in computational sensors.

MOSIS offers two monthly runs of a standard 2um, double-layer metal, CMOS process. One of these runs usually includes a second layer of polysilicon. Typically these designs are fabricated, bonded and returned in about two months. In addition to these standard

runs, a 1.2um CMOS run goes out about once every month and there are more infrequent runs at 0.8um. Every other month includes a low-noise 2um analog CMOS run which has options for second poly, a NPN bipolar transistor in the n-well, and a buried channel CCD.

MOSIS's capability, however, is limited for the research and development of computational sensors. Quality bipolar and depletion-mode MOS devices are unavailable. MOSIS is beginning to offer GaAs (instead of the more usual Silicon) process runs on a regular basis.

At this point, MOSIS does not provide a capability for optical electronics fabrication. University researchers must rely on teaming with industries which have the fabrication capability in this area. It is noteworthy that both the European research community and the Japanese micro-sensor project will have a common facilities including capabilities for optical electronics fabrication.

4.6 Education, Workshops/Networking and Literature

Understanding semiconductor and device physics as well as techniques for marketing custom-made integrated circuits are essential prerequisites to developing a successful computational sensor. For the complete success of a computational sensor, avenues of communication between VLSI designers, computer vision researchers, and product developers must be developed. These groups would exchange information about the opportunities and difficulties in each others' fields. Vision (and other sensor) researchers must be made aware of what is available in VLSI technology, and VLSI designers must understand the problems of machine vision. This workshop was very productive. It was recommended that follow-on workshops or conferences be held.

It was proposed that universities and industries team-up to allow students to obtain more hands-on experience. This is an old idea that still has difficulty working in practice. Namely, most students and university professors are more likely to undertake theoretical research than to work on the "real thing". This is primarily due to the fact that dealing with hardware tends to extend time in graduate school for students, and reduce the publishing rate of professors. This problem received some attention, and reviews of academic standards were suggested. It was suggested that more credit should be given to efforts which produce working prototype devices or systems.

The body of experience and knowledge of computational sensors is currently scattered over a large number of disciplines and corresponding publications. Publications range from journals on electronic circuits and signal processing to publications on neural networks and vision research. To effectively communicate knowledge about computational sensors, it was suggested that a new journal be created.

Another type of cooperation is to distribute working prototype sensors in among the user community. An excellent example is the log-polar camera prototype that University of Pennsylvania has offered to share with interested researchers. This type of cooperation is of mutual benefit to the sensor designers as well as to application developers. Designers of the computational sensor receive much needed feedback about the actual need and practical value of the sensor, while application researchers can investigate new areas previously limited by the absence of these specialized devices.

5 Recommendations

In light of the previous analysis, the workshop has recommended the following:

1. Create a research and development program in computational sensors. The program must have the following characteristics (Figure 1):
   - Interdisciplinary - the program must include sensing, algorithms, VLSI, material, and applications;
   - Multi-modal - the program must deal with not only the image or visual modality, but also with other sensing modalities including tactile, acoustic, pressure, acceleration, chemical, and so on;
   - Prototyping-oriented - individual projects under this program must be oriented toward producing working prototype devices or systems;
   - Applications - individual projects must identify potential applications and possible avenues of technology transfer to real world applications.
2. Improve the infrastructure for research and development of computational sensors:
   - Fabrication facilities - MOSIS (or similar facilities) must be expanded to include technologies for optical and mechanical sensor development;
   - Tools - Tools for designing and testing computational sensors can be far more complicated, than they are for standard VLSI design. Standardization, and library and tool development are essential;
   - Education - Hands-on experience must be provided to graduate students;
   - Networking and workshops - Researchers in computational sensors, by its nature, are scattered in multiple fields, and mechanisms; workshops and consortiums must be developed to bring them together.

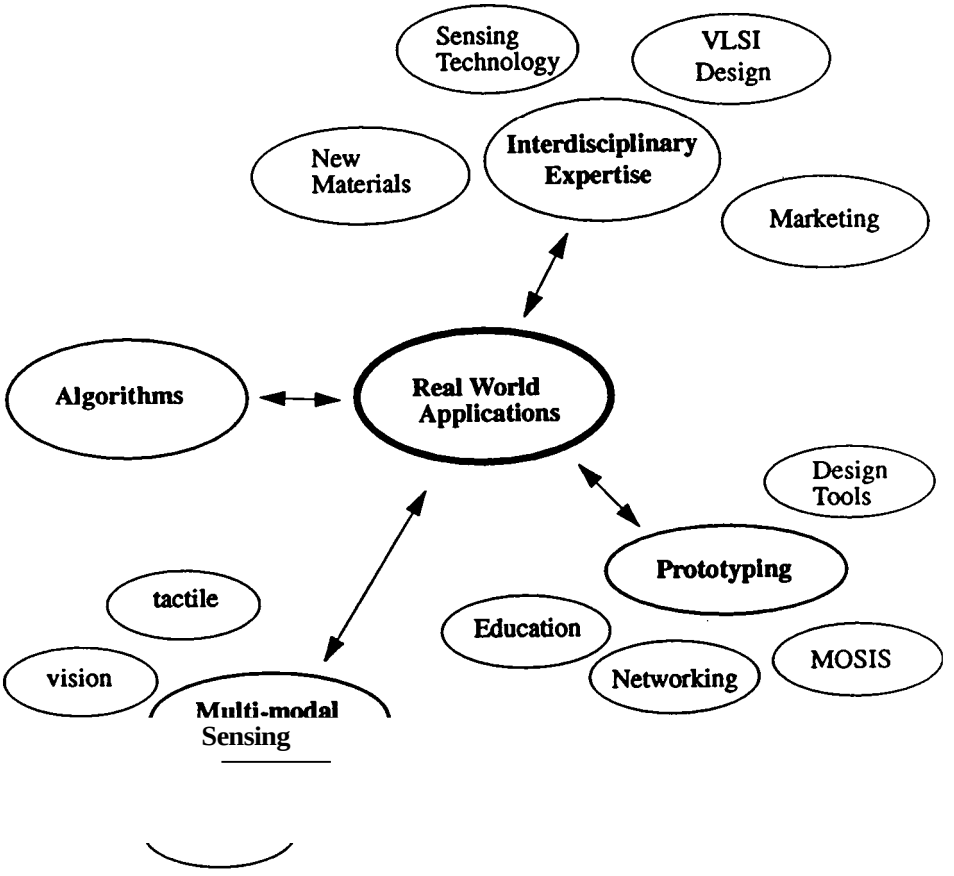

Figure 1: **Computational Sensor** Program

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