

largest noise figure and much stronger frequency dependence, while device C shows the smallest NF and slight frequency dependence. There was a great improvement in the noise figure of the device when metal 1 grounded shielding was used. The results are similar to those of BJTs [5]. After the probe pad parasitics were de-embedded, the NFs of the three devices improved and became much closer to that of other devices. The dependence of the NFs on frequency also decreased especially for device C. The small difference between the de-embedded NFs is presumably caused by imperfect de-embedding. This requires further study of the de-embedding procedures [6–8]. The NFs of devices A, B and C before de-embedding at 2.4 GHz were 3.1, 2.0 and 0.7 dB, and those after de-embedding were 1.2, 0.8 and 0.5 dB, respectively. Device C exhibited the best noise performance and the smallest difference in NF before and after de-embedding. The results also demonstrate that device C, metal 3 with grounded metal 1 shielding, has the most appropriate pad structure for obtaining the intrinsic noise figure characteristics of MOSFETs. Moreover, the intrinsic NF of a MOSFET having the same pad structure as device C can be approximately obtained without any de-embedding procedure as the frequency is < 3 GHz.

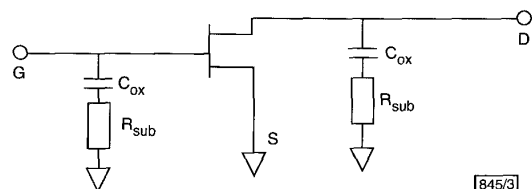


Fig. 3 Equivalent circuit model of MOSFET with GSG probe pads

To explain the different NF behaviours before de-embedding the pad parasitics, we used parasitic equivalent circuits of the dummy GSG probe pads, similar to those of [9]. Fig. 3 shows a simplified equivalent model of the MOSFET with GSG probe pads and Table 1 the extracted equivalent circuit parameters, parasitic oxide capacitance (C_{ox}) and parasitic substrate resistance (R_{sub}). The value of R_{sub} falls from 244.8 Ω in the case of device B to 11.8 Ω in the case of device C, and are lightly dependent on the frequency because a certain amount of parasitic substrate capacitance (C_{sub}) neglected in Fig. 3 exists in the substrate. Since the noise characteristics relate to the resistive impedance, we believe that a reduction in the value of R_{sub} for device C results in an improvement in the noise performance and makes the least difference before and after de-embedding.

Table 1: Extracted equivalent circuit parameters

Device	A	B	C
C_{ox} [fF]	192	78.8	138.3
R_{sub} [Ω]	234.8	244.8	11.8

Conclusions: The effect of substrate parasitic resistance on the noise figure performance of MOSFETs has been evaluated by measuring the noise figures of devices with different coplanar GSG probe pad structures. The equivalent parasitic circuit models of the different GSG probe pads were proposed. The improvement in the noise figure of a device with grounded metal 1 shielding is probably be due to the reduction in the parasitic substrate resistance. The top level metal used in modern deep submicron CMOS technology is recommended for realising the GSG probe pads and bottom level metal as the grounded shielding to obtain the best noise figure performance.

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Light-sensitive CMOS ring oscillator

N.D. Jankovic and V. Brajovic

A simple light-sensitive CMOS ring oscillator, the oscillation frequency of which depends on the chip ambient illumination, is presented. An experimental 21-stage ring oscillator fabricated in 0.5 μ m CMOS changes the pulse frequency from 50 Hz in total darkness to 2 MHz in extreme bright ambient at $V_{dd} = 1$ V.

Introduction: A standard CMOS ring oscillator (RO) consists of a self-oscillating chain of odd number inverters connected in a feedback loop. As a voltage-controlled oscillator, it is commonly used for analysing CMOS gate dynamic characteristics [1]. Recently, Boyle *et al.* proposed a modified current-controlled RO circuit operating as on-chip temperature sensor [2].

In this letter, we describe a light-sensitive RO circuit the oscillation frequency of which depends on the average ambient illumination.

Circuit description: An electrical schematic diagram of the novel light-sensitive inverter forming the RO chain is shown in Fig. 1. Two P^+ / N_{well} photodiodes (PDs) control the charging and the discharging time of the input gate capacitance of both the PMOSTs and MMOSTs. For instance, when the input voltage is high, the PMOST is quickly turned off by the forward-biased PD D_1 . The charging time of the NMOST gate is much longer, since it is controlled by the D_2 inverse leakage current $I_r = I_{dark} + I_{photo}$, where I_{dark} is the diode dark current and I_{photo} is the light generated photo-current. As a consequence, the PMOST is turned off before the NMOST gate potential achieves the threshold voltage V_{th} .

Since the same effect also occurs when the input voltage is low, the PMOST and the NMOST are effectively never in the on-state simultaneously. This efficiently eliminates the inverter's short-circuit current and decreases the total RO power consumption.

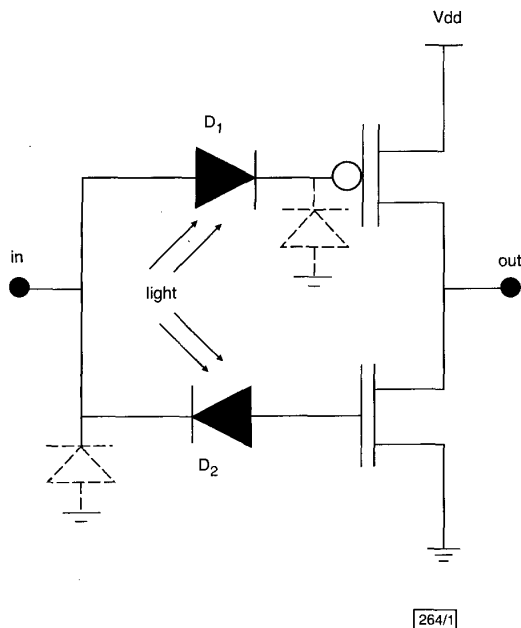


Fig. 1 Basic inverter circuit of light sensitive ring-oscillator (RO)

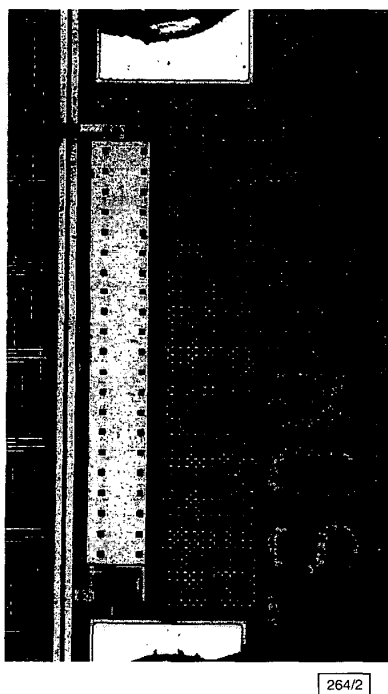


Fig. 2 Photo-micrograph of fabricated RO

Metal 3 layer stripe covers all 21 inverters except output buffer. $3 \times 3 \mu\text{m}$ holes in Metal 3 are located above P^+/N_{well} photodiodes

The transition delay time of a light-sensitive inverter is the sum of the gate charging time and MOST turn-on time. Assuming fully matched active devices in Fig. 1, the resulting RO frequency $F[\text{Hz}]$ may be expressed as

$$F[\text{Hz}] = \frac{1}{2N \left\{ \frac{v_{th} c_{gs}}{I_r} + \frac{c_l}{k g_m} \right\}} \quad (1)$$

where N is the number of inverters, c_{gs} is the gate-source input capacitance, c_l is the load capacitance of the next inverter stage (including the diode and line capacitance), g_m is the MOS transistor transconductance and k is a constant ($k \sim 2.7$). Eqn. 1 shows that, at high illumination, a linear sensitivity will be maintained as long as the gate charging time is much longer than the MOST turn-on time, which yields the condition $I_r \ll g_m V_{th} c_{gs} / k c_l$. This condition may not hold at high chip illumination due to the excessive generation of I_{photo} . It can be avoided, however, by minimising the layout of the PD and/or by using various light filters. At low illumination, $F[\text{Hz}]$ becomes fully proportional to I_r . In this case, a linear sensitivity is preserved if $I_{photo} \gg I_{dark}$. Since I_{dark} is proportional to the PD depletion region volume, it appears that a minimum PD layout design maximises an RO linear sensitivity range at both high and low chip illumination levels.

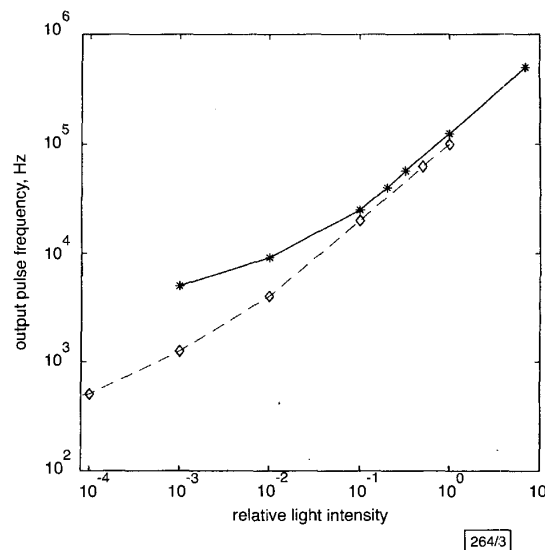


Fig. 3 Measured RO frequency against relative light intensity for 1.3 and 1V power supply V_{dd}

* $V_{dd} = 1.3\text{V}$
 ◇ $V_{dd} = 1\text{V}$

The two parasitic $N_{\text{well}}/P_{\text{subs}}$ PDs, plotted in Fig. 1 by dashed lines, also appear in the inverter design. They are, however, less effective in generating photo-current since most of the photon flux is already absorbed by the main P^+/N_{well} PDs. A parasitic PD, which is attached to the gate of the PMOST, operates in parallel with D_1 during the PMOST gate charging period. It shortens the low-to-high transition time of the inverter and increases the RO output pulse signal duty cycle slightly above 50%. The other parasitic PD is connected to the cathode of D_2 and has no meaningful influence on the RO frequency.

Experimental results and discussion: A test 21-stage light-sensitive RO with output buffer was designed and fabricated in $0.5 \mu\text{m}$ N_{well} CMOS with silicide block capability via MOSIS. Following given design roles, two identical P^+/N_{well} photodiodes of each inverter were laid out as a minimum allowed P^+ diffusion in a minimal N_{well} area. A final light-sensitive inverter layout including a minimum-size CMOS transistor pair occupied a $30 \times 10 \mu\text{m}$ silicon area. A micro-photograph of the fabricated RO with the output buffer is shown in Fig. 2. As seen, a Metal 3 layer was used as the light shield with $3 \times 3 \mu\text{m}$ openings only above the areas of the PD. The measured dependencies of the RO frequency against relative light intensity for 1.3 and 1V voltage supplies are shown in Fig. 3. During the measurements, an open package with mounted RO chip faced a white board illuminated by a constant diffused light. Kodak Wratten neutral gelatin filters were used to vary the chip illumination. Note that the light intensity of 1 on the x-scale of Fig. 3 approximately corresponds to average room illumination. The results in Fig. 3 indicate a linear RO light sensitivity of more than two orders of magnitude change in chip illumination. When V_{dd} was changed from 1.3 to 1V, the linear range extended towards lower light intensities. As explained previously, this can be attributed to a decrease in I_{dark} with scaling V_{dd} . In full dark-

ness (chip covered), the lowest measured RO frequencies were 830Hz and 50Hz for 1.3 and 1V power supplies, respectively. For very high chip illumination, however, a slow output buffer in our present design limits the maximum frequency to ~2MHz for a full output voltage swing. A standard 21-stage RO without PDs oscillated at 33MHz, as found by SPICE simulation.

In conclusion, we have described a fully CMOS compatible light-sensitive ring oscillator featuring linear frequency sensitivity over a wide range of chip ambient illumination. This circuit may be used as an on-chip light-sensitive clock generator or as a stand-alone 1V battery-operated light detector.

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InGaAs quantum dot lasers with sub-milliamp thresholds and ultra-low threshold current density below room temperature

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Continuous-wave operation of InGaAs quantum dot lasers is studied. A very low threshold current of 460µA is achieved at 200K for a 5µm × 1170µm oxide-confined stripe laser. For a larger stripe width of 11µm, a threshold current density of 5.2A/cm² is demonstrated. The characteristic threshold temperature is ~700K in the temperature range of 140-200K, and drops rapidly around room temperature.

Since the pulsed [1] and continuous-wave (CW) [2, 3] demonstrations of 1.3µm quantum dot (QD) lasers, recent attention has focussed on fully utilising the potential of QD lasers for low threshold operation [4]. In this Letter, we show that these QD lasers have potential for extremely low threshold current and current density. The room temperature characteristics of the devices are presently limited by heating [5] and do not fully reveal the remarkable potential of QD lasers for low power operation. Here, however, we show the potential for low threshold for lower temperature operation slightly below room temperature. For a 5µm × 1170µm oxide-confined stripe laser at 200K, the CW lasing threshold current is as low as 460µA with a threshold current density of 7A/cm². For a stripe width of 11µm, the threshold current density is even lower at ~5A/cm². From 140 to 200K the characteristic temperature for CW operation is 700K. In addition, we discuss how to extend this type of extremely low threshold to room temperature.

The QD edge-emitting laser structure is grown using molecular beam epitaxy. A schematic illustration of the laser is shown in the inset of Fig. 1. The guiding layer is 0.188µm thick undoped Al_{0.05}Ga_{0.95}As, and the cladding layers are 2µm thick Al_{0.85}Ga_{0.15}As containing 300Å thick Al_{0.98}Ga_{0.02}As oxidation layers. The QD active region is grown on 15 monolayers of In_{0.10}Ga_{0.90}As placed at the centre of the guiding layer. The detailed heterostructure and growth parameters are described elsewhere [3, 4].

As shown in Fig. 1, the lasers are fabricated from a ridge structure by wet etching passing through the lower oxidation layer. Wet oxidation at 470°C for 4mins [6, 7] forms aperture widths

between 5 and 11µm along the ridge structure. Devices with 1.17mm cavity length are formed by cleaving. High reflectivity coatings are applied to both end facets. After processing, the devices are mounted on copper and tested CW over temperatures ranging from 140 to 300K. The lasing transition is obtained from the ground energy levels of the QD ensemble for all measurement temperatures.

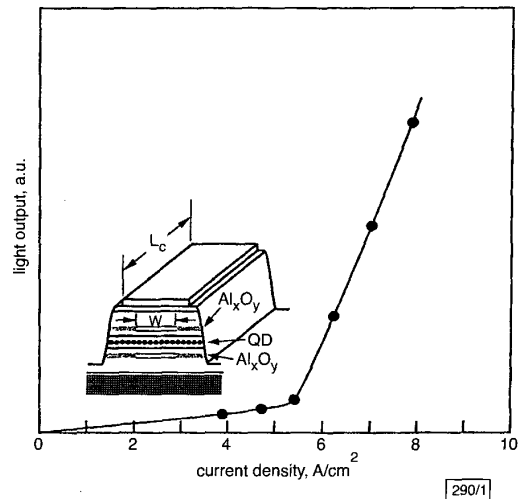


Fig. 1 Light against current density at 140K and threshold current density of 5.2A/cm²

1.3µm QD edge emitter

11µm × 1170µm

HR/HR, CW

Inset: schematic illustration of device cross-section

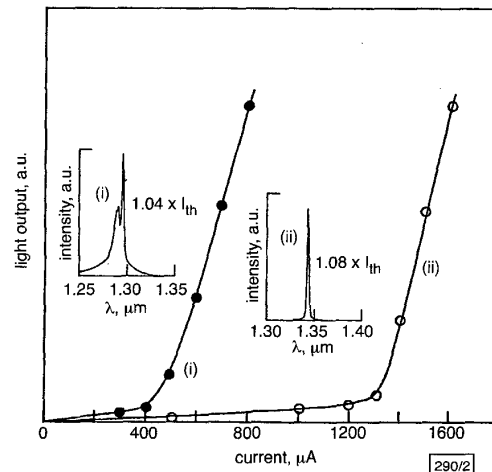


Fig. 2 Light against current at 200 and 300K and threshold current of 460µA at 200K and 1.3mA at 300K

(i) $T = 200\text{K}$, $I_{th} = 460\mu\text{A}$

(ii) $T = 300\text{K}$, $I_{th} = 1.3\text{mA}$

1.3µm QD edge emitter

5µm × 1170µm

HR/HR, CW

Insets: lasing spectra at wavelengths of 1.30 and 1.34µm at each temperature

Fig. 1 shows the light against current density curve for an 11µm wide device at 140K. A very low threshold current density of 5.2A/cm² is obtained. To our knowledge, this is the lowest threshold current density ever reported for a semiconductor laser operating at this or higher temperatures. The transparency current density of the QD active region is given by $J_{trans} = qn_{QD}/\tau_{sp}$, where n_{QD} ($\approx 1.5 \times 10^{10}\text{cm}^{-2}$) is the QD density and τ_{sp} is the average lifetime. We estimate that $\tau_{sp} \approx 600\text{ps}$ at this temperature [8], and that the transparency current is ~4A/cm².

Fig. 2 shows the light against current curve and lasing spectra for a 5µm wide stripe at 200 and 300K. At 200K, the threshold