16.7 100frames/s CMOS Range Image Sensor

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Triangulation–based light stripe methods are the most practical and quite robust for range imaging [5]. In a previously-proposed high-speed triangulation approach [6], the laser in the triangulation imaging setup is continuously swept across the scene. Each pixel in the sensor "sees" the laser stripe only once as it sweeps across its line of sight. By recording the time when a particular pixel sees the laser, the range for each pixel can be determined. Implementation of this cell-parallel technique is reported in References 7 and 8. However, the triangulation method is inherently row-parallel: only one pixel in each given row sees the laser stripe at any given time. The row-parallel architecture employing a winner–take–all (WTA) circuit embedded in each row of the sensor reported here enables most of the circuitry of References 7 and 8 to be removed from pixels and reused once per row at the edge of the array.

The sensor optically receives an image, the WTA selects an absolute intensity peak in each row, and reports the location and magnitude of the selected peak. Figure 16.7.1 shows the location and magnitude of the winner, reported by the WTA, as the bright laser line travels across the row of 20 photodetectors. The positive peaks occur when the laser is centered on the photodetector. The negative peaks occur when the laser is exactly between two photodetectors 0. Locating peaks (positive and negative) allows precise localization of the laser at the spatial grid that is twice the spatial resolution of the photodetector grid.

The row–parallel architecture of the sensor is shown in Figure 16.7.2. The WTA circuits continuously localize the laser stripe in each row and generate voltage waveforms similar to one shown in the bottom graph of Figure 16.7.1. One-per-row peak detectors monitor these voltages. When the peak detector detects either a positive or a negative peak in a particular row, it latches the time stamp in one-per-row memory. The row memories are rapidly scanned to ensure that no new peaks occur before the information regarding the most recent peak has been read out. When the scanner selects a row, the output current of the WTA is multiplexed to the position encoder together with the type of the peak (i.e., positive or negative). Time information, together with the address and the peak type, provides all the information needed for the reconstruction of the range map. Figure 16.7.3 shows a range map collected with the current 64x64 prototype. The ultimate speed of the sensor is above 100frames/s, while the depth resolution is estimated at 1mm from about 1.5mm viewing distance. The chip micrograph is shown in Figure 16.7.7.

Figure 16.7.4 shows one pixel. Transistors M4 and M5 form one cell of a current mode WTA circuit 00 fed with the photocurrent as an input. The WTA is slow for small input currents requiring a boost to achieve high frame rates 0. To boost the photocurrent while ensuring good matching, BJT Q1 is used as a photodetector. Transistors M1 and M2 form classic regulated cascode for minimizing voltage swings on the base thereby minimizing the waste of tiny photocurrent (Iph) on charging and discharging base collector junction. In this way, all of the photocurrent is immediately available for the amplification in the BJT and subsequent WTA processing thereby improving the dynamic response of the circuit. The emitter junction needs to swing to establish appropriate Vbe to pass emitter current $Ie = (1+\beta)Iph$. The assumption is that the Ie is much larger than Iph due to β. Therefore, Ie can afford to charge and discharge emitter node. Unfortunately for small photocurrents, β is close to unity. Instead of a simple BJT, we have employed a so-called vertical inversion-layer emitter pnp BJT structure 0. The cross-section of such MOS-bipolar four-terminal device is shown in Figure 16.7.5. The entire internal base surface potential of the vertical p+/nwell/psubs BJT is controlled by the MOS gate potential Vg. The main advantage of such an MOS-controlled BJT acting as the phototransistor is high β maintained even at low collector currents Ic. It is attributed to the suppression of the minority-carrier surface recombination at the n-well (base) by forming the p-type inversion layer over the entire internal base surface when $Vg>Vtp$ 0. The drawback is the large emitter capacitance due to the added MOS capacitor that may render the regulated cascode loop M1-M2 unstable.

Bootstrapping with a 2Vgs level shifter, as shown in Figure 16.7.4, eliminates the unwanted effects. Since β varies with Vg, a magnitude of the generated Ie for fixed illumination may be also controlled by Vg. Measured Ie vs. Vg characteristics for various relative light illumination of grounded-collector vertical pnp MOS-BJT are shown in Figure 16.7.6. In this test, the emitter is kept constant at $1.2V$. The maximum Ie is achieved around $Vg=-0.25V$ at which the nwell surface potential acquires p-channel threshold voltage $Vtp = Vg-Vbe-Ve = -0.85V$. Beyond that point, Ie saturates because the channel-to-base potential difference is pinned by the forward biased p+/nwell diode and, consequently, further decrease of Vg has no further influence on β. This effect is used in the bootstrapping technique. The base potential is pinned by the feedback. The bootstrapping 2Vgs level shifter ensures that the photogate is sufficiently below the base potential $(2Vgs-Vbe)>Vtp$, thus overdriving the photogate to fully establish the inversion layer. Small potential variations conveyed from the emitter to the photogate do not cause β to change since the circuit is deeply in the region where β saturates (the leftmost region in Figure 16.7.6). The level shifter M3 allows enough headroom for the $2Vgs$ buffer.

References:

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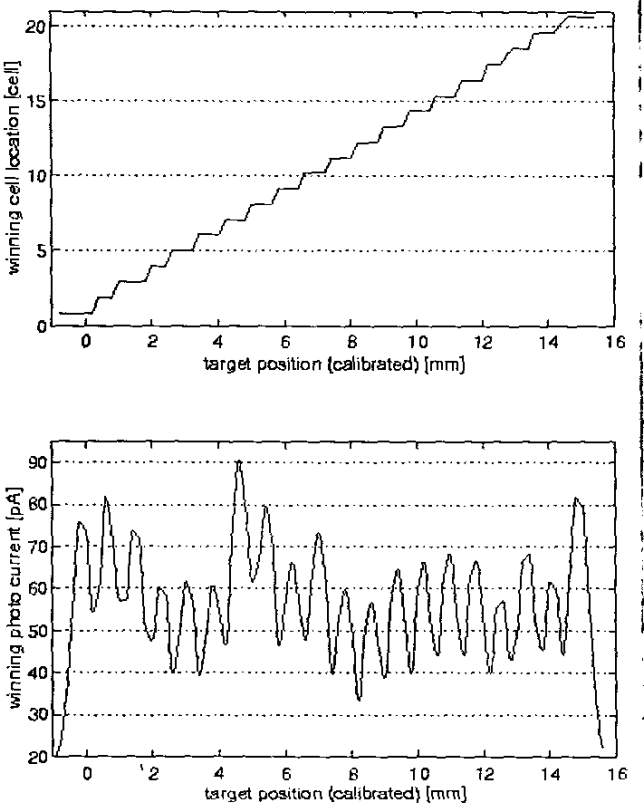

Figure 16.7.1: Identification and magnitude of the winning input with a WTA circuit.

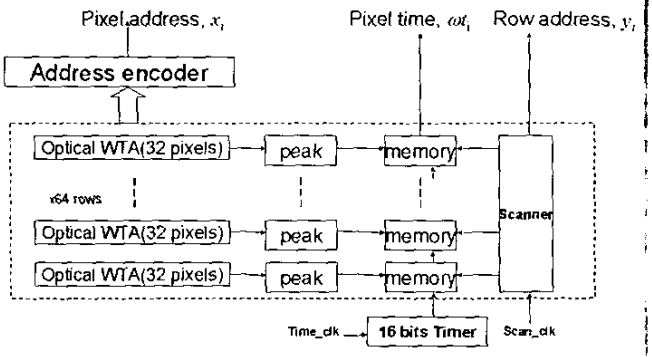

Figure 16.7.2: Row-parallel architecture of the sensor.

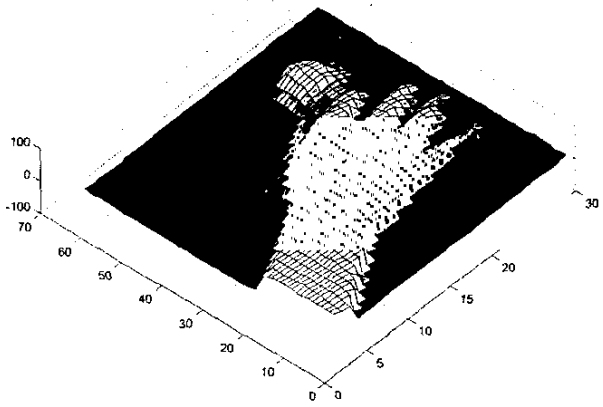

Figure 16.7.3: Range map example.

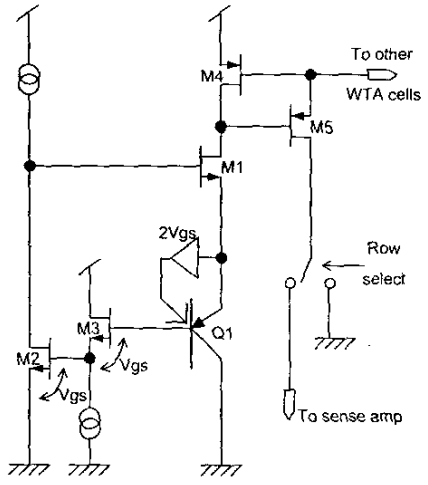

Figure 16.7.4: Pixel schematic.

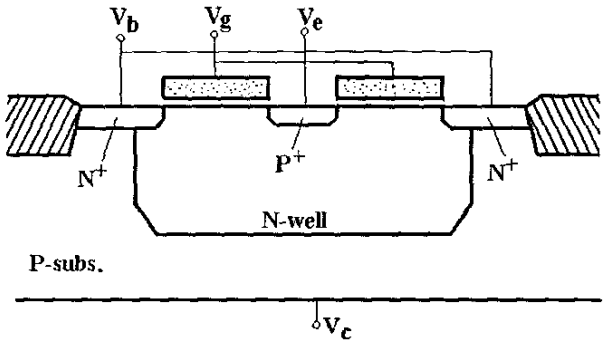

Figure 16.7.5: High β vertical pnp MOS-BJT.

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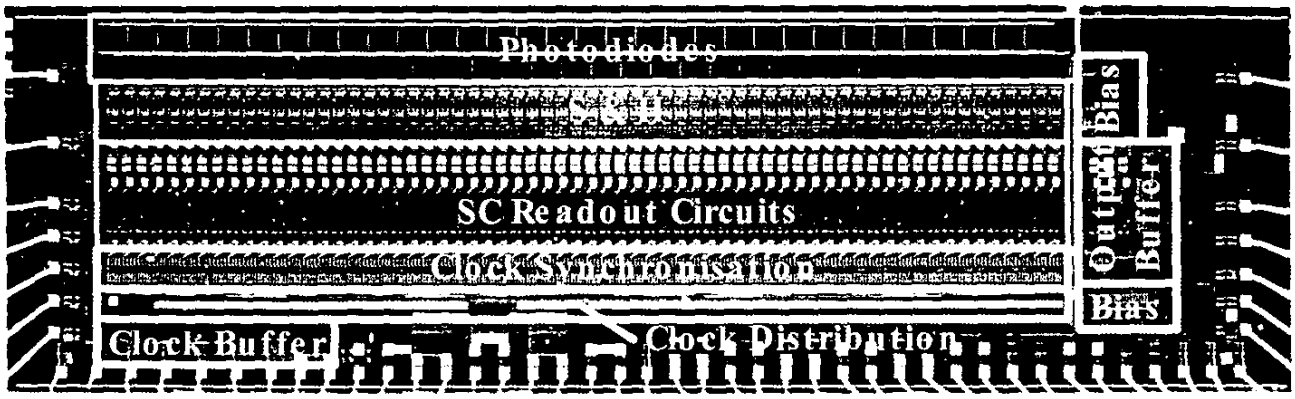

Figure 16.5.7: 3D image sensor chip micrograph.

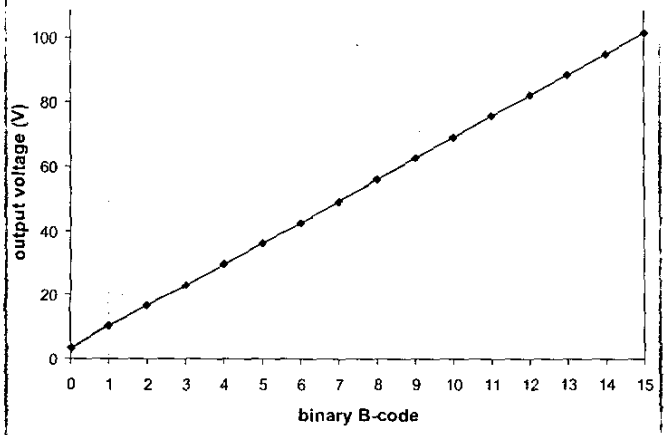

Figure 16.6.7: The generator's output voltage vs. the 4-bit input data word.

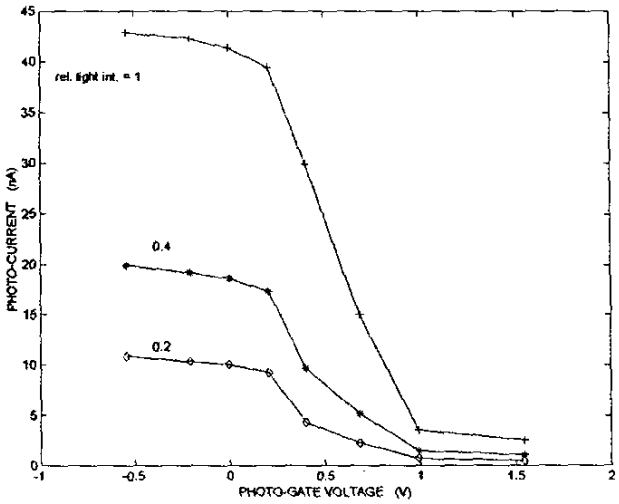

Figure 16.7.6: BJT gain bust with photogate biasing.

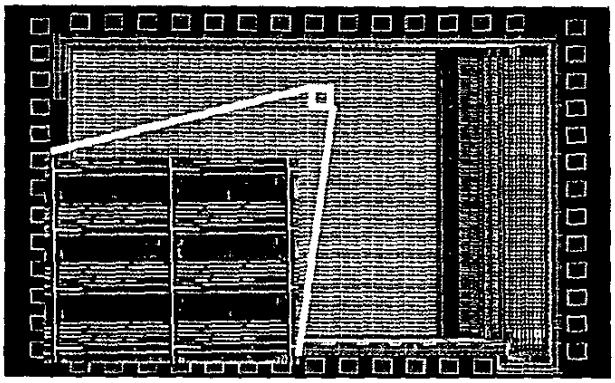

Figure 16.7.7: Range sensor layout with 6 enlarged pixels.

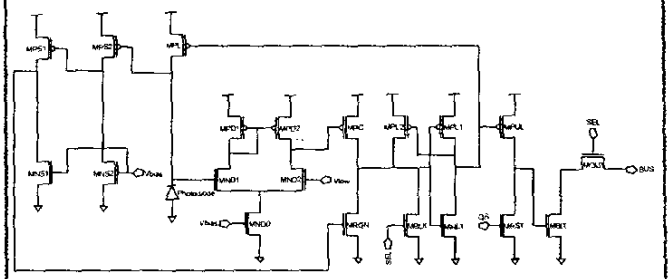

Figure 17.1.5: A diagram of the pixel-parallel photocurrent-controlled oscillator circuit used for A/D conversion.